

PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 5367-256PUS	
<p>I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]</p> <p>on _____</p> <p>Signature _____</p> <p>Typed or printed name _____</p>		Application Number 10/590,744	
		Filed May 17, 2007	
		First Named Inventor Marco FRIEDRICH	
		Art Unit 2835	
		Examiner PATEL, Ishwarbhai B.	
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>			
I am the			
<input type="checkbox"/> applicant/inventor.		<u>/Alfred W. Froebrich/</u> Signature	
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)		<u>Alfred W. Froebrich</u> Typed or printed name	
<input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>38,887</u>		<u>(212) 687-2770</u> Telephone number	
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____		<u>May 23, 2011</u> Date	
<p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>			
<input type="checkbox"/> *Total of _____ forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Arguments/Comments

Independent claim 1 stands rejected as obvious in view of US 6,860,620 (Kuan). The Examiner's rejection relies on the statement that a larger area provides better heat removal. The Examiner's sole reliance on this statement is in error because (1) the statement ignores that additional material increases the cost and (2) Kuan teaches that a thickness of the layers is a result effective variable. Thus, without the benefit of hindsight afforded by the Applicant's disclosure there is no reason that one skilled in the art would increase the area to achieve the conductive layer occupying at least 60% of a plane of the circuit board based on Kuan and what is known to those skilled in the art.

Independent claim 1 recites "a flexible circuit board comprising electrical conductor tracks and a thermally conductive layer", "wherein the thermally conductive layer and the electrical conductor tracks are positioned in a same plane of the flexible circuit board", and "wherein the thermally conductive layer occupies at least 60 % of an area of said same plane."

The Examiner acknowledges that Kuan fails to disclose that the thermally conductive layer occupies at least 60% of an area of said same plane. However, the Examiner simply reasons that a bigger area is better because a bigger area would provide better heat removal. More specifically, the Examiner states in the Advisory Action dated February 25, 2011 that it would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the circuit board of Kuan with maximum possible heat removal area. However, this statement by the Examiner simply ignores the fact that more material means higher manufacturing costs. A person skilled in the art at the time of the invention would design a heat removal area of a printed circuit board to be as large

as necessary to remove the heat generated by the components to be mounted on the printed circuit board, and no more. See, for example, col. 3, lines 60-64, of Kuan, which clearly indicates that cost is a design factor. Thus, one skilled in the art would not simply make the heat sink as large as possible.

Furthermore, Kuan discloses an arrangement in which the heat sink tracks are rectilinear and are arranged between rectilinear electrical conductor tracks. Therefore, the arrangement of the heat sink tracks is limited to the space between the electrical tracks. The space between the electrical tracks in Kuan is not 60% of the plane of the circuit board on which the conductor tracks are arranged. MPEP 2144.05(II)(B) states that a particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. In fact, Kuan discloses at col. 3, lines 55-60, that within the context of the configuration of Kuan, the thickness of the layer affects the heat sink capabilities.

Further, MPEP 2143 states that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396. Here the Examiner is combining the teaching of Kuan with the general statement that a bigger thermally conductive layer is better. Only the present invention presents a different configuration of the electrical conductor tracks and thermally conductive layer that allows the thermally conductive layer to occupy at least 60% of an area on the circuit board. The inventors made this configuration so that the circuit board could accommodate high power light emitting diodes while maintaining a relatively small

circuit board. Based on the teachings of Kuan, there is no reason that one skilled in the art would have made an area of the heat sink layer to be at least 60% of the same layer in which the electrical conductors are arranged.

For all of the above reasons, the rejection of claim 1 in view of Kuan should be withdrawn.

Regarding dependent claim 12, the Examiner's rejection of this claim includes another error because the Examiner simply states that providing a solder mask is old and well known and that it would have been obvious to provide Kuan with an insulating layer containing a soldering mask, while the upper layer of the tracks disclosed by Kuan are made of gold, an inert material that does not require protection by a solder mask. Further, an additional layer, such as an insulating layer, applies to Kuan contradicts the object of Kuan of providing a thin arrangement. Accordingly, there is no reason that one skilled in the art would provide an insulating layer to Kuan's device without hindsight knowledge gained from the present application.

For all of the above reasons, the Examiner's rejections of the claims of the present invention in view of Kuan should now be withdrawn.